ABSTRACT OF THE DISCLOSURE

A packet switch includes an input buffer memory unit having a logic queue corresponding to an output line, a control module for a first pointer indicating a scheduling start input line, a control module for a second pointer indicating a scheduling start output line of scheduling target outlines, a request management control module for retaining transmission request data about a desired output line, a scheduling processing module for starting a retrieval from within plural pieces of transmission request data from the output line indicated by the second pointer, and selecting an output line that is not ensured by other input lines, a packet buffer memory unit for temporarily storing a plurality of fixed-length packets and sequentially outputting the fixed-length packets, a switch unit for switching the fixed-length packets outputted from the packet buffer memory unit, and an address management unit for segmenting an address of the packet buffer memory unit into fixed-length blocks for a plurality of packets, and managing the address on a block basis. With this construction, the memory address is managed on the block basis, and a memory capacity can be reduced by giving an intra-block individual address per queue when in writing or reading.